P25C08H_Auto

Automotive 8-Kbit Serial SPI bus EEPROM

Datasheet Rev.1.3

General Description

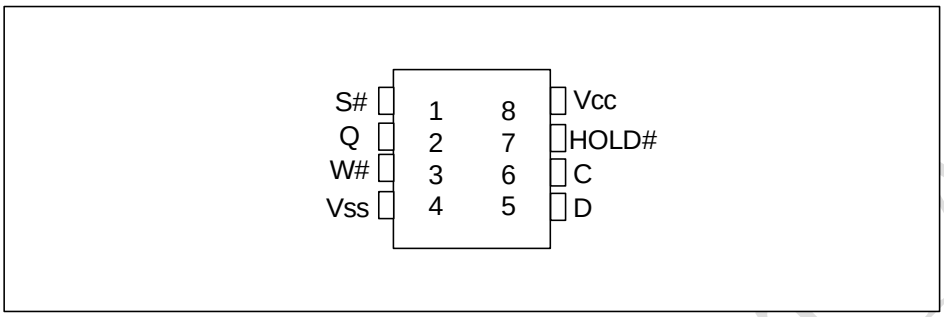
The P25C08H is Serial Peripheral Interface (SPI) compatible EEPROM (Electrically Erasable Programmable Memory) Automotive grade device operating up to 125°C. The P25C08H contains a memory array of 8 Kbits (1 Kbytes), which is organized in 32 bytes per page. It is compliant with the Automotive standard AEC-Q100 grade 1.

Features

- AEC-Q100 qualified
- Single supply voltage: 1.7 V to 5.5 V
- Max clock frequency:
  - 15MHz clock from 4.5 V to 5.5 V
  - 5MHz clock from 1.7 V to 5.5 V
- Serial Peripheral Interface (SPI) Compatible
  - Standard SPI: C, S#, D, Q, W#, HOLD#
  - Mode 0 and Mode 3
- Memory array
  - 8 Kbits of EEPROM
  - Page size: 32 bytes
- Write
  - Byte/Page Write within 5ms
- Hardware Controlled Locking of Protected Sectors by WP Pin
- Transparent ECC on each group of four bytes which can correct 1 bit error
- High Reliability
  - Endurance: 4 Million Write Cycles(25C)
  - Data Retention: 200 Years
  - HBM: 6 kV
  - Latch up Capability: +/- 200mA(125C)
- Package: SOP8, TSSOP8, UDFN8

1. Pin Configuration

1.1 Pin Configuration



SOP8/TSSOP8/UDFN8

1.2 Pin Definition

Table 1-1 Pin Definition for SOP8/TSSOP8/UDFN8 Packages

Pin	Name	Type	Description
1	S#	Input	Chip Select
2	Q	Output	Serial Data Output
3	W#	Input	Write Protect
4	Vss	Ground	Ground
5	D	Input	Serial Data Input
6	C	Input	Serial Clock
7	HOLD#	Input	Hold
8	V_{CC}	Power	Power Supply

1.3 Signal Description

During all operations, VCC must keep stable and within the specified valid range: VCC (min) to VCC (max). All the input and output signals must keep high or low according to voltages of VIH, VOH, VIL or VOL, as specified in: DC and AC parameters. These signals are described next.

1.3.1 Serial Data Output (Q)

This output signal is used to transmit data sequentially into the device. Data is shifted out on the falling edge of Serial Clock (C).

1.3.2 Serial Data Input (D)

This output signal is used to transmit data sequentially into the device. It receives instructions, addresses, and the data to be recorded. Values are latched on the rising edge of Serial Clock (C).

1.3.3 Serial Clock (C)

This input signal provides the serial interface timing. The instructions, addresses, or data present in the Serial Data Input (D) are glued on the rising edge of Serial Clock (C). The data on the Serial Data Output (Q) changes at the lower edge of Serial Clock (C).

1.3.4 Chip Select (S#)

During the signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. The device will be in the Standby Power mode, only when an internal Write cycle is in progress. Driving Chip Select (S#) low selects the device, placing it in the Active Power mode.
After power-up, a falling edge on Chip Select (S#) is required before beginning instruction.

1.3.5 Hold (HOLD#)

The Hold (HOLD#) signal is used to pause any serial communications with the device without deselecting the device.
During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.
To start the Hold condition, you must select the device, with driven low of Chip Select (S#).

1.3.6 Write Protect (W#)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).
This pin must be driven either high or low, and must be stable during all Write instructions.

1.3.7 VCC supply voltage

V_{cc} is the supply voltage.

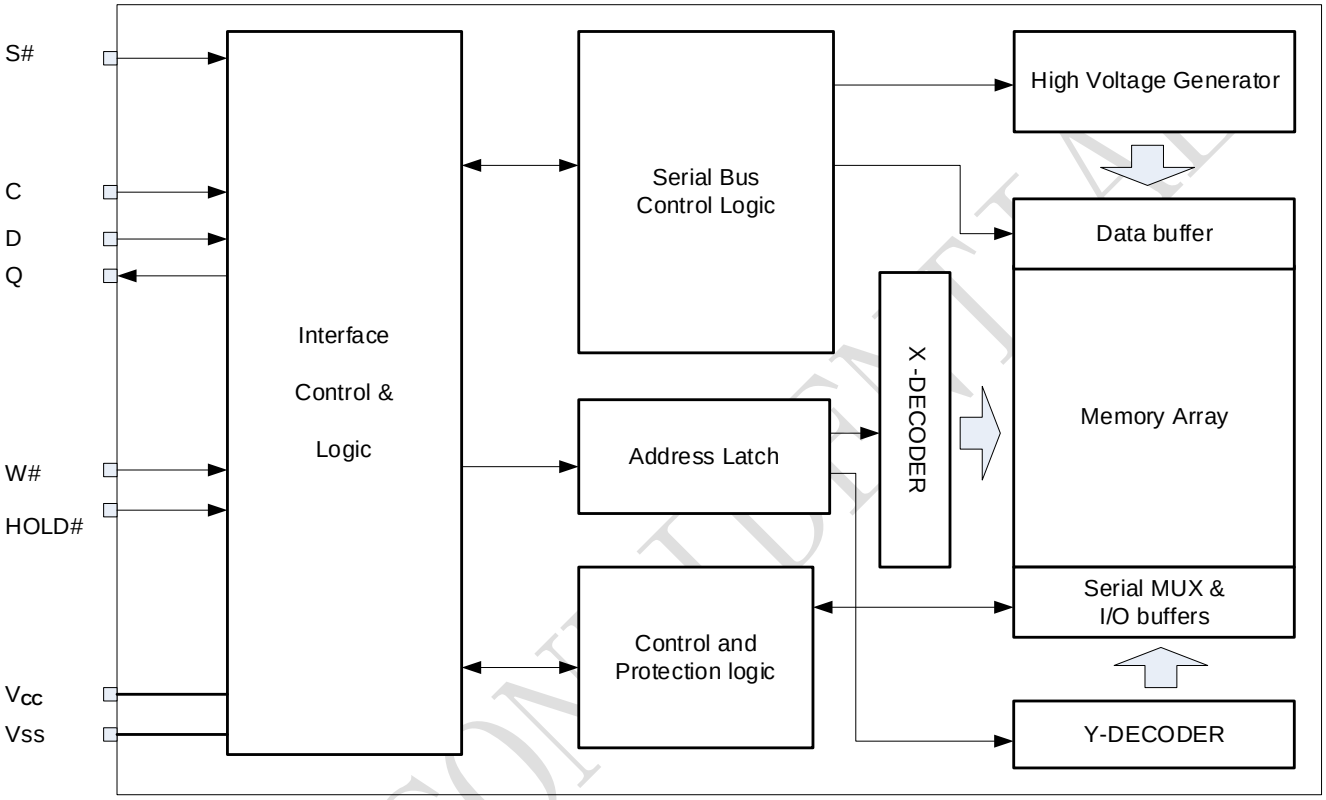
1.3.8 VSS ground

Vss is the benchmark for all signals, including voltage supply V_{cc}.

2. Block Diagram

The memory is organized as shown in the following figure

Figure 2-1 Block Diagram

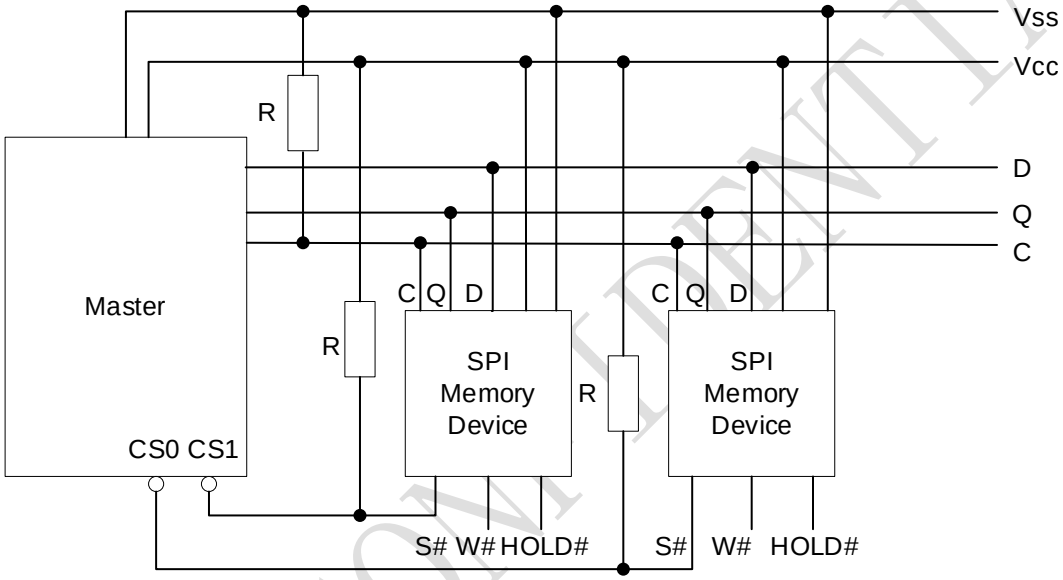


3. Connecting to the SPI bus

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select (S#) goes low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 3-1 The master and memory devices on the SPI bus



Note:
1.The Write Protect (W#) and Hold (HOLD#) signals should be driven, high or low as appropriate.

Figure 3-1 shows an example of two memory devices connected to an SPI bus master. Only one memory device is selected, so only one memory device drives the Serial Data Output (Q) line at a time. The other memory devices are high impedance.
The pull-up resistor R (represented in Figure 3-1) ensures that a device is not selected if the Master leaves the S line in the high impedance state.
In applications where the Master keeps all SPI bus lines simultaneously high impedance (for example, if the Master is reset during an instruction transmission), the clock line (C) must be connected to an external pull-down a resistor that ensures the C line is pulled low (While S# line is pulled high) when all inputs / outputs are high impedance: this ensures that S and C do not go high at the same time and tSHCH Is guaranteed to meet the requirements. The typical value for R is 100kΩ.

3.1 SPI Modes

When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode

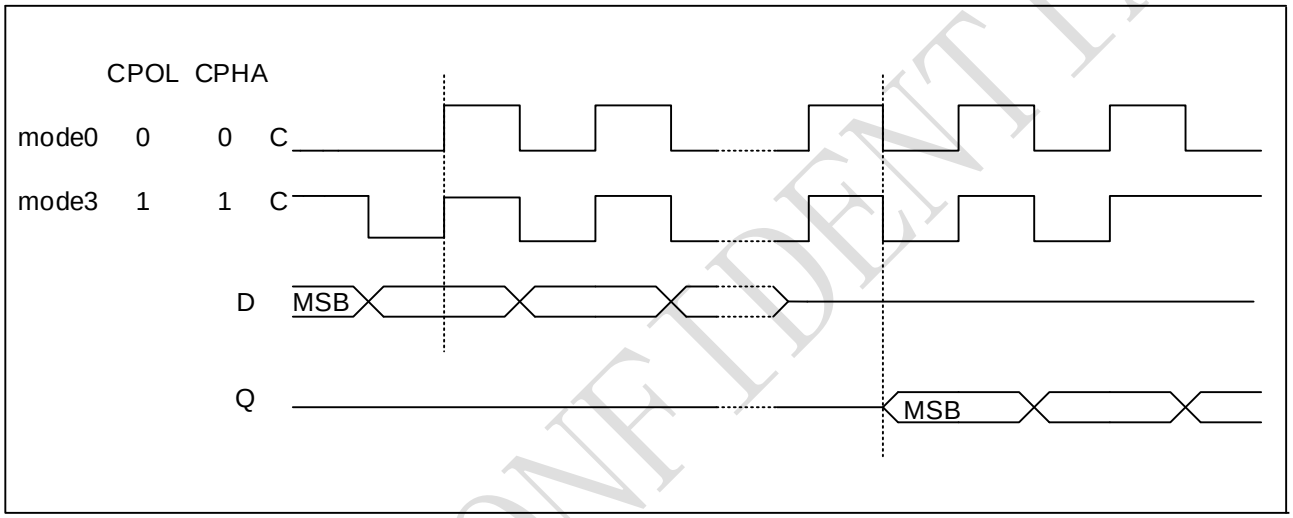
until next S# falling edge. In standby mode, Q pin of this LSI should be High-Z. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next S# rising edge.

Input data is latched on the rising edge of Serial Clock (C) and data shifts out on the falling edge of C The difference of serial peripheral interface mode 0 and mode 3 is shown as Figure 3-2:

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

- CPOL = 0, CPHA = 0
- CPOL = 1, CPHA = 1

Figure 3-2 SPI modes supported



Note:
CPOL indicates clock polarity of serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which serial mode is supported.

4. Electrical Characteristics

Table 4-1 Absolute Maximum Ratings [1]

Symbol	Parameter	Min.	Max.	Units
T_{STG}	Storage Temperature	-65	150	°C
T_A	Ambient operating temperature	-40	125	°C
V_{CC}	Supply Voltage	-0.5	6.5	V
V_{IO}	Input or output range	-0.5	6.5	V
I_{OL}	DC output current	-	5	mA

Note: [1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4-2 Pin Capacitance

Symbol	Parameter	Max.	Units	Test Condition [1]
C_{OUT}	Output capacitance (Q)	8	pF	V_{OUT} = 0 V
C_{IN}	Input capacitance (D)	6	pF	V_{IN}= 0 V
	Input capacitance (other pins)	6	pF	V_{IN}= 0 V

Note: [1].Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 5 MHz

Table 4-3 DC Characteristics （Unless otherwise specified, VCC = 1.7V to 5.5V, TA = –40°C to 125°C）

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{CC}	Supply Voltage	1.7	-	5.5	V	
Isb	Standby Current	-	0.6[2]	5.0	μA	V_{CC} =5.5V, Vin = Vss or V_{CC} Ta=85℃
		-	-	20.0	μA	V_{CC} =5.5V, Vin = Vss or V_{CC} Ta=125℃
I_{CC1}[1]	Supply Current(read)	-	0.3[3]	1.0	mA	V_{CC} = 3.3 V, Q=open, C = 0.1 V_{CC} / 0.9 V_{CC} at 5 MHz
			0.6[4]	2.0	mA	V_{CC} = 5.5 V, Q=open, C = 0.1 V_{CC} / 0.9 V_{CC} at 5 MHz
I_{CC2}[1]	Supply Current(write)	-	-	3.0	mA	V_{CC} =5.5V, Ta=85℃
I_{LI}	Input Leakage Current	-	-	±2.0	μA	V_{IN} = V_{CC} or Vss
I_{LO}	Output Leakage Current	-	-	±2.0	μA	V_{OUT} = V_{CC} or Vss
V_{IL}	Input Low Level	-0.45	-	0.3V_{CC}	V	1.7 V ⩽ V_{CC} ⩽5.5V
V_{IH}	Input High Level	0.7V_{CC}	-	V_{CC}+0.5	V	1.7 V ⩽ V_{CC} ⩽5.5V
V_{OL}	Output Low Level	-	-	0.3	V	I_{OL} = 0.15 mA, V_{CC} = 1.8 V
V_{OH}	Output high voltage	0.8V_{CC}	-	-		I_{OH} = –0.1 mA, VCC = 1.7 V

Note: [1] Characterized values, not tested in production

[2] Typ. ISB @ VCC =5.5V, T_A =25℃

[3] Typ. ICC1 @ VCC =3.3V, T_A =25℃

[4] Typ. ICC1 @ VCC =5.5V, T_A =25℃

Table 4-4 AC Characteristics （Unless otherwise specified, VCC = 1.7V to 5.5V, TA = –40°C to 125°C, CL=30pF, Test Conditions are listed in Notes [2] ）

Symbol	Parameter	1.7≤V_{CC}≤5.5			4.5≤V_{CC}≤5.5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_C	Clock frequency	DC	-	5	DC	-	15	MHz
t_{SLCH}	S active setup time	60	-	-	15	-	-	ns
t_{SHCH}	S not active setup time	60	-	-	15	-	-	ns
t_{SHSL}	S deselect time	90	-	-	30	-	-	ns
t_{CHSH}	S active hold time	60	-	-	15	-	-	ns
t_{CHSL}	S not active hold time	60	-	-	15	-	-	ns
t_{CH}	Clock high time	80	-	-	20	-	-	ns
t_{CL}	Clock low time	80	-	-	20	-	-	ns
t_{CLCH}	Clock rise time	-	-	2	-	-	2	us
t_{CHCL}	Clock fall time	-	-	2	-	-	2	us
t_{DVCH}	Data in setup time	20	-	-	5	-	-	ns
t_{CHDX}	Data in hold time	20	-	-	10	-	-	ns
t_{HHCH}	Clock low hold time after HOLD# not active	60	-	-	15	-	-	ns
t_{HLCH}	Clock low hold time after HOLD# active	60	-	-	15	-	-	ns
t_{CLHL}	Clock low set-up time before HOLD# active	0	-	-	0	-	-	ns
t_{CLHH}	Clock low set-up time before HOLD# not	0	-	-	0	-	-	ns
t_{SHQZ}	Output disable time	-	-	80	-	-	20	ns
t_{CLQV}	Clock low to output valid	-	-	80	-	-	20	ns
t_{CLQX}	Output hold time	0	-	-	0	-	-	ns
t_{QLQH}	Output rise time	-	-	80	-	-	20	ns
t_{QHQL}	Output fall time	-	-	80	-	-	20	ns
t_{HHQV}	HOLD# high to output valid	-	-	80	-	-	20	ns
t_{HLQZ}	HOLD# low to output high-Z	-	-	80	-	-	20	ns
t_W	Write time	-	-	5	-	-	5	ms

Notes:

[1] tCH + tCL must never be lower than the shortest possible clock period, 1/fC(max).

[2] Characterized only, not tested in production.

Table 4-5 Reliability Characteristic [1]

Symbol	Parameter	Test condition	Min.	Unit
EDR[2]	Endurance	TA ≤ 25 °C, VCC(min) < VCC < VCC(max)	4,000,000	Write cycles
		TA = 85°C, VCC(min) < VCC < VCC(max)	2,000,000	
		TA = 125°C, VCC(min) < VCC < VCC(max)	1,000,000	
DRET	Data retention	TA = 55 °C	200	Years
		TA = 85 °C	100	
		TA = 125 °C	50	

Note:

[1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 3.3V, Page mode

Figure 4-1 Serial input timing

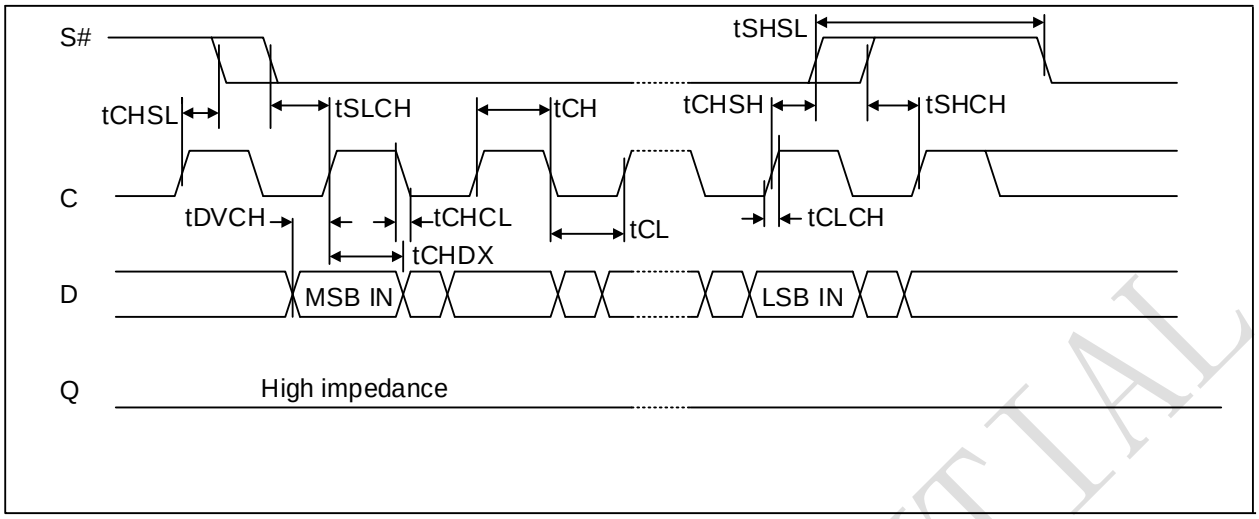


Figure 4-2 HOLD# timing

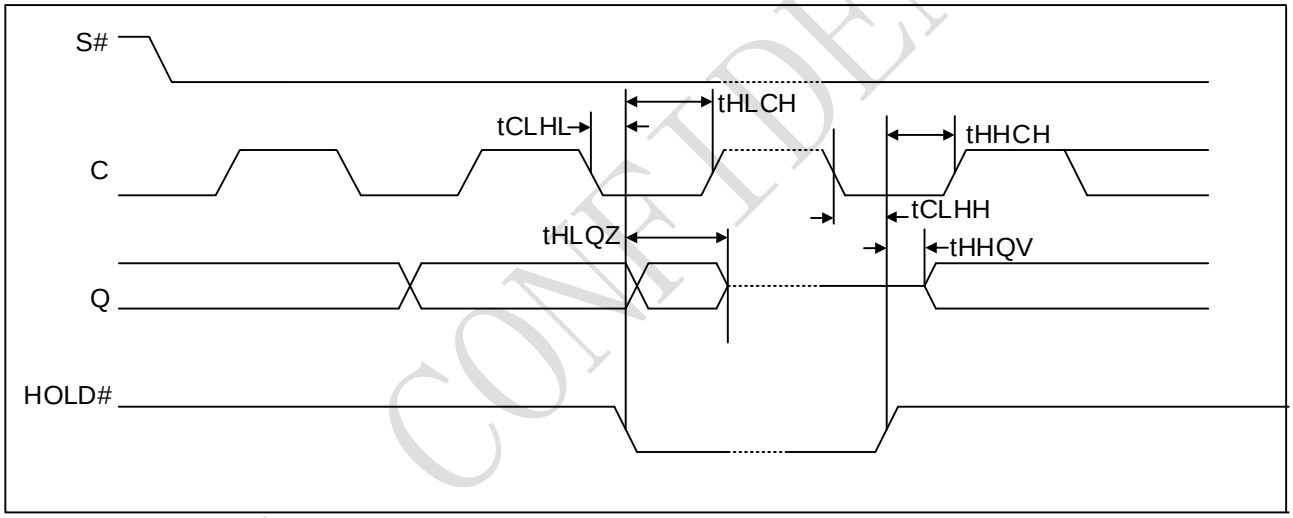
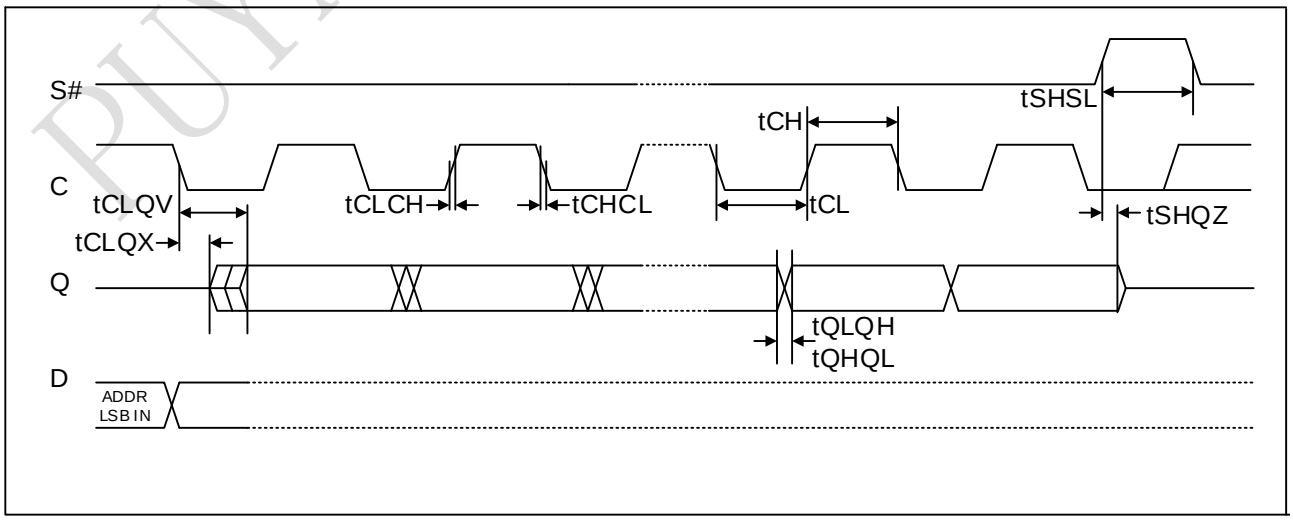


Figure 4-3 Serial output timing

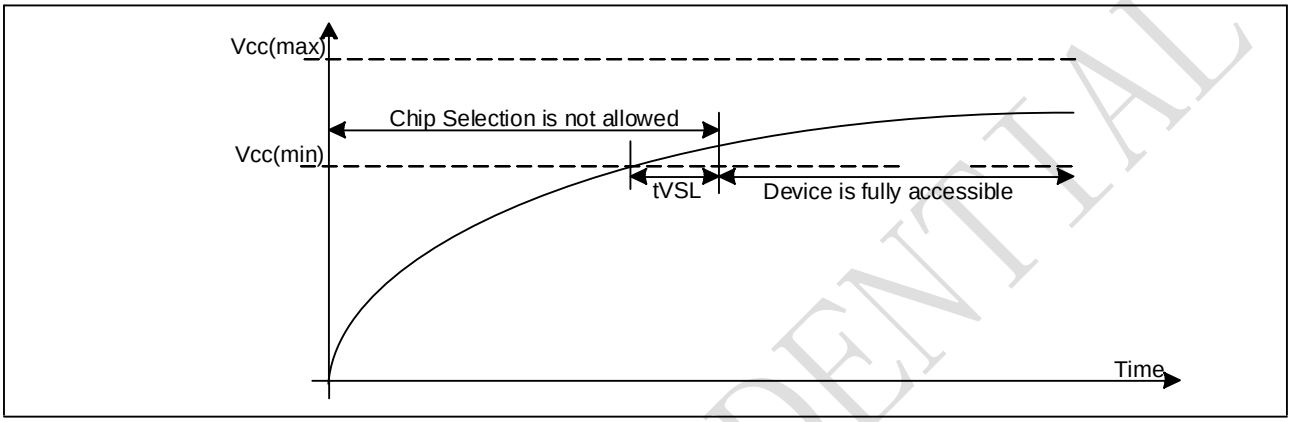


Device Power-Up

The EEPROM has a built-in power-on-reset circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-reset circuit normally, the following conditions must be satisfied to raise the power supply voltage.

When initialization is successfully completed by the power-on-reset circuit, the EEPROM enters the standby status. tVSL is the time required to initialize the EEPROM. No instructions are accepted during this time.

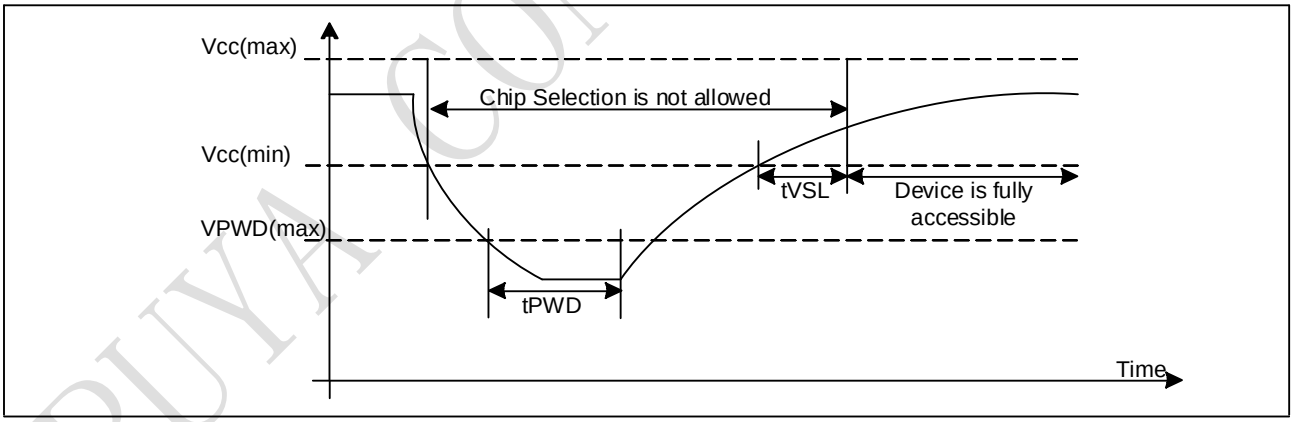
Figure 4-4 Power up Timing



Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the V_{cc} of EEPROM device must below VPWD for at least tPWD timing. Please check the table below for more detail.

Figure 4-5 Power down-up Timing



Symbol	Parameter	min	max	unit
VPWD	V_{cc} voltage needed to below VPWD for ensuring initialization will occur		0.7	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	V_{cc} (min.) to device operation	100		us
tVR	V_{cc} Rise Time	1	500000	us/V

5. Operating features

5.1 Supply voltage (VCC)

5.1.1 Operating supply voltage (V_{CC})

Before selecting memory and issuing a command, an effective and stable V_{CC} voltage must be applied within the specified range [V_{CC}(min), V_{CC}(max)] (see operating conditions in DC and AC parameters). This voltage must remain stable and valid until the end of the instruction transfer and for a write instruction until the end of the internal write cycle (tW). To ensure a stable DC supply voltage, it is recommended to disconnect the V_{CC} line with a suitable capacitor (usually between 10 and 100 nF) near the V_{CC}/ Vss device pins.

5.1.2 Device reset

In order to prevent erroneous instruction decoding and inadvertent Write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} reaches the POR threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage.

At power-up, when V_{CC} passes over the POR threshold, the device is reset and is in the following state:

- in Standby mode
- deselected
- Status Register values:
  - ✧ The Write Enable Latch (WEL) bit is reset to 0.
  - ✧ The Write In Progress (WIP) bit is reset to 0.
  - ✧ The SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits).

It is important to note that the device must not be accessed until V_{CC} reaches a valid and stable level within the specified [V_{CC} (min), V_{CC} (max)] range, as defined under Operating conditions.

5.1.3 Power-up conditions

After powering on, V_{CC} will continuously increase from Vss to V_{CC}. During this time, the Chip Selection line (S #) does not allow to float, and the V_{CC} voltage must be followed. Therefore, it is recommended that the S-line be connected to V_{CC} by proper tensile strength.

In addition, the Chip Select (S#) input offers a built-in safety feature, as the S input is edge-sensitive as well as level-sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select (S#). This ensures that Chip Select (S#) must have been high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined under Operating conditions. After the Min. V_{CC} operation voltage, user has to wait 100us, then the chip can operation normally.

5.1.4 Power-down

During power-down (continuous decrease of the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined under Operating conditions), the device must be:

- deselected (Chip Select S# should be allowed to follow the voltage applied on V_{CC}),
- in Standby mode (there should not be any internal write cycle in progress).

5.2 Active Power and Standby Power modes

When Chip Select (S#) is low, the device is selected, and in the Active Power mode. The device consumes ICC.

When Chip Select (S#) is high, the device is deselected. If a Write cycle is not currently in progress, the device then goes into the Standby Power mode, and the device consumption drops to ICC1, as specified in DC characteristics.

5.3 Hold condition

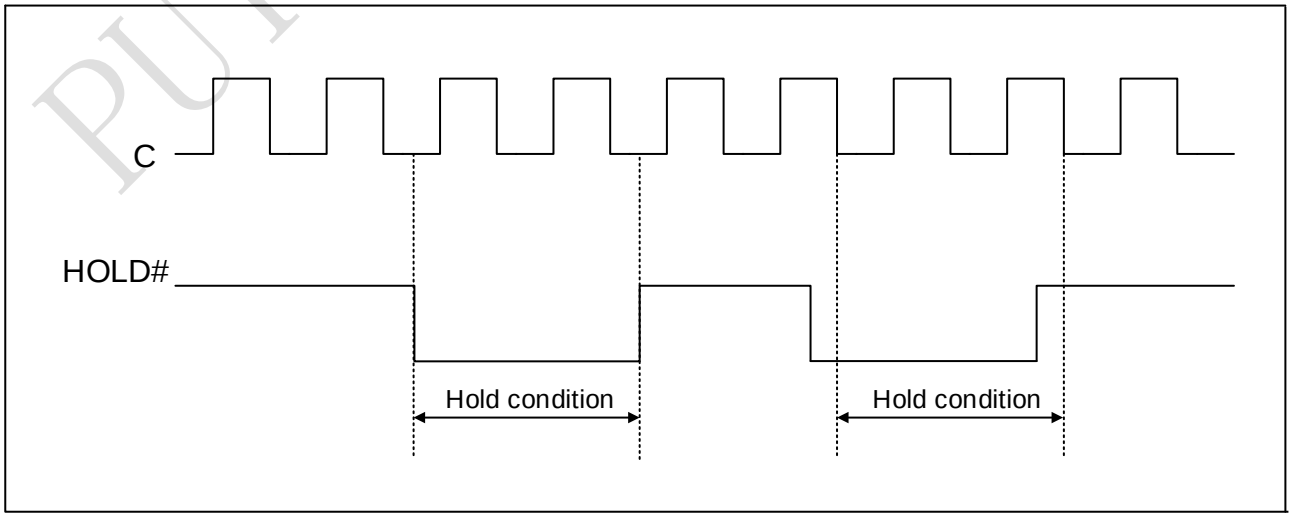
HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, writing in progress.

The operation of HOLD requires Chip Select (S#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (C) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock (C) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low).

During the Hold condition, the Serial Data Output (Q) is high impedance, and the Serial Data Input (D) and the Serial Clock (C) are Don't Care.

Normally, the device is kept selected for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition has the effect of resetting the state of the device: this mechanism can be used, if required, to reset the ongoing processes [1] [2].

Figure 5-1 Hold condition activation



The Hold condition starts when the Hold (HOLD#) signal is driven low when Serial Clock (C) is already low (as shown in Figure 5-1).

Figure 5-1 also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being low.

Note：

1. This resets the internal logic, except the WEL and WIP bits of the Status Register.
2. In the specific case where the device has moved in a Write command (Inst + Address + data bytes, each data byte being exactly 8 bits), deselecting the device also triggers the Write cycle of this decoded command.

5.4 Data protection and protocol control

The device has the following data protection mechanisms:

- Before accepting the execution of the Write and Write Status Register instructions, the device checks whether the number of clock pulses comprised in the instructions is a multiple of eight.
- The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, write command is accepted.
- The Block Protect (BP1, BP0) bits in the Status Register are used to configure part of the memory as read-only.
- The Write Protect (W#) signal is used to protect the Block Protect (BP1, BP0) bits in the Status Register.
- For any instruction to be accepted, and executed, Chip Select (S#) must be driven high after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C).
- Two points should be noted in the previous sentence:
- The “last bit of the instruction” can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The “next rising edge of Serial Clock (C)” might (or might not) be the next bus transaction for some other device on the SPI bus.

Table 5-1 Write-protected block size

BP1	BP0	Blocks	Protected array addresses
0	0	None	None
0	1	Upper quarter	0300h – 03FFh
1	0	Upper half	0200h – 03FFh
1	1	Whole memory	0000h – 03FFh

6. Instructions

Each command is composed of bytes (MSB bit transmitted first), initiated with the instruction byte, as summarized in Table 6-1.

If an invalid instruction is sent (one not contained in Table 6-1), the device automatically enters in a Wait state until deselected.

Table 6-1 Instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

For read and write commands to memory array and Identification Page the address is defined by two bytes as explained in Table 6-2.

Table 6-2 Significant bits within the address bytes (1) (2)

Instruction	Upper address byte								Lower address byte							
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
READ or WRITE	x	x	x	x	x	x	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Note:

1. A: Significant address bit

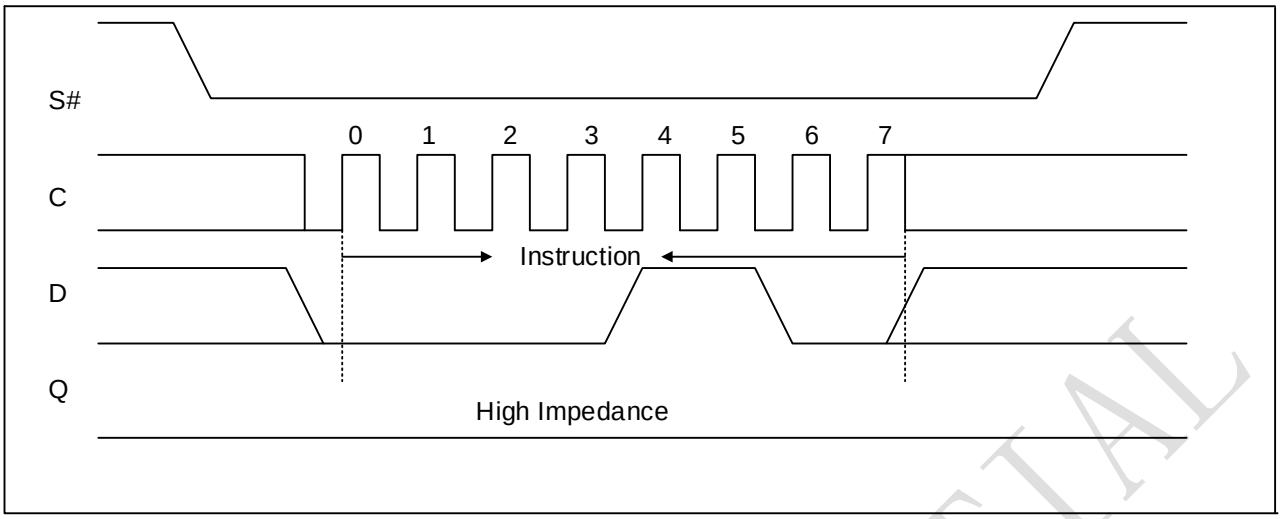
2. x: bit is Don't Care

6.1 Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like WRITE.WRSR and WRID which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

As shown in Figure 6-1, the sequence of issuing WREN instruction is: S# goes low→ sending WREN instruction code→ S# goes high.

Figure 6-1 Write Enable (WREN) sequence



6.2 Write Disable (WRDI)

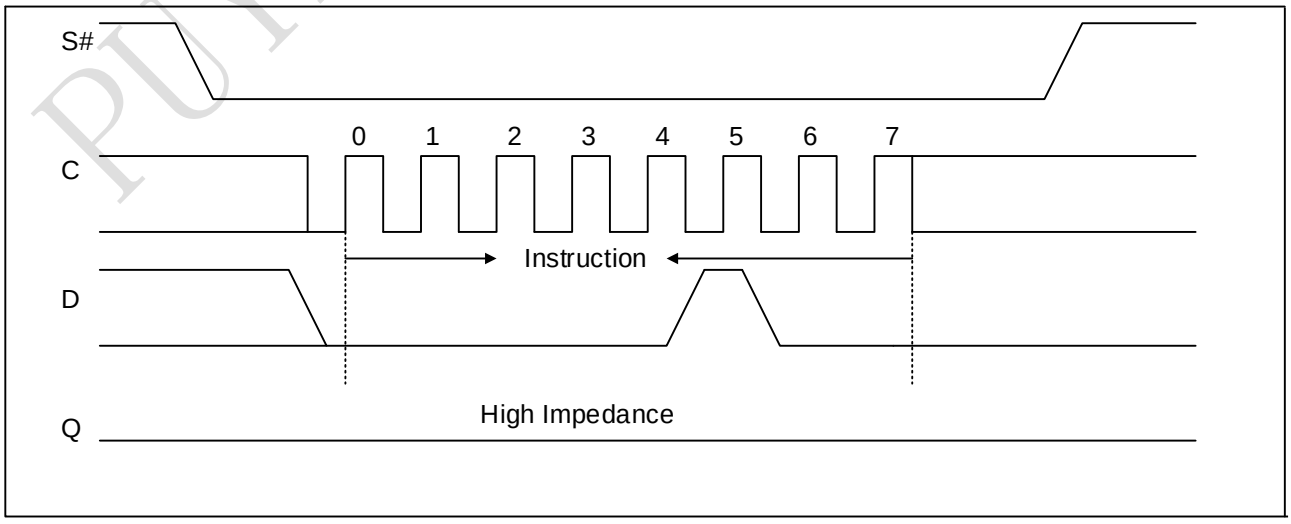
The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

As shown in Figure 6-2, the sequence of issuing WRDI instruction is: S# goes low→ sending WRDI instruction code→ S# goes high.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRID instruction completion
- WRITE instruction completion.

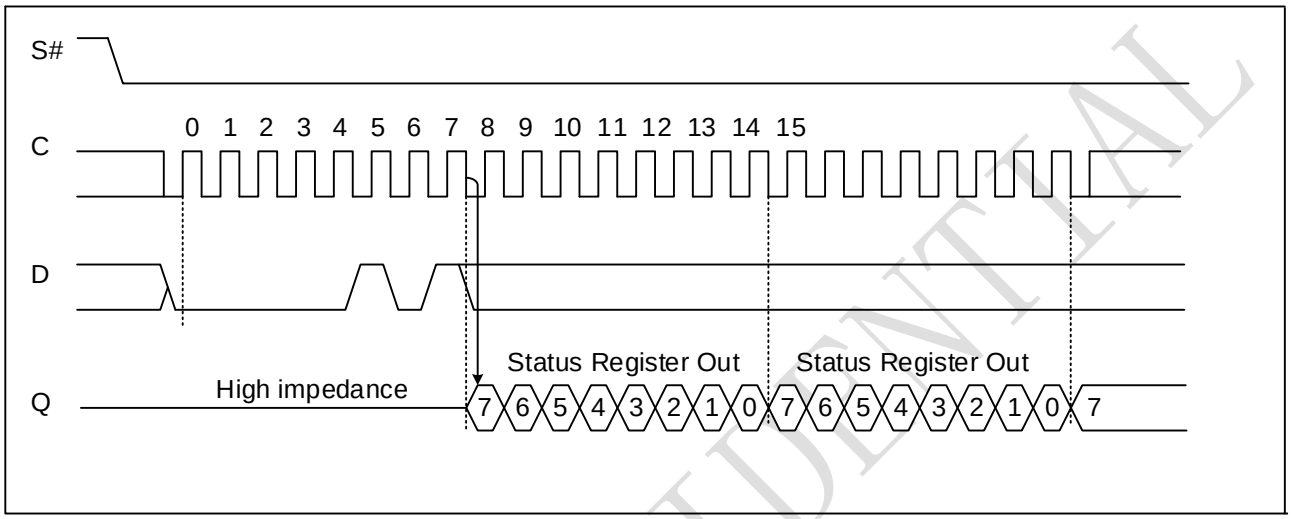
Figure 6-2 Write Disable (WRDI) sequence



6.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction is used to read the Status Register. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 6-3.

Figure 6-3 Read Status Register (RDSR) sequence



6.3.1 WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0, no such cycle is in progress.

6.3.2 WEL bit

When set to 1, the internal Write Enable Latch is set. When set to 0, the internal Write Enable Latch is reset, and no Write or Write Status Register instruction is accepted.

The WEL bit is returned to its reset state by the following events:

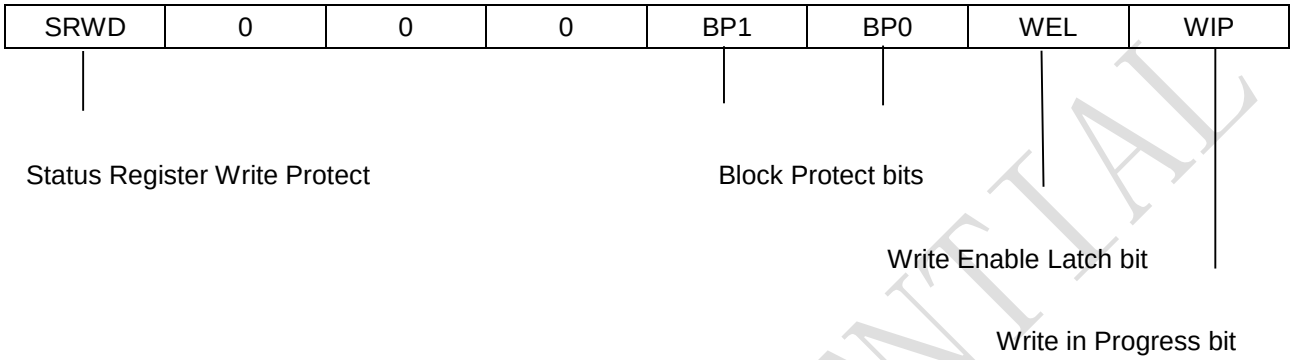
- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Write (WRITE) instruction completion

6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are nonvolatile. They define the size of the area to be software-protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 5-1) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

6.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect (W#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W#) signal enable the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect (W#) is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

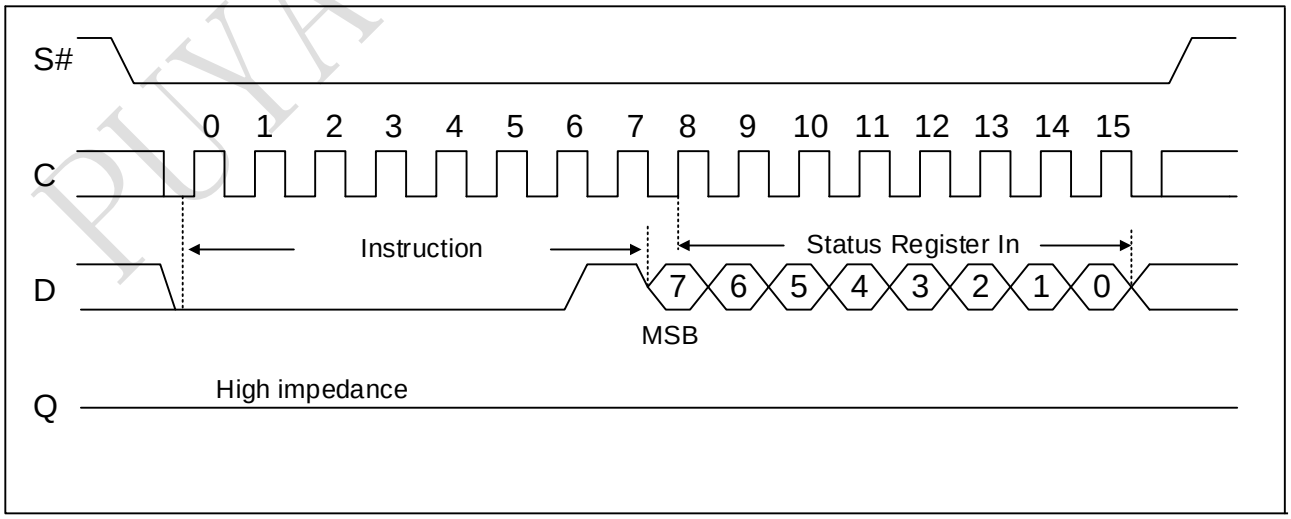


6.4 Write Status Register (WRSR)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The instruction sequence is shown in Figure 6-4. The sequence of issuing WRSR instruction is: S# goes low → sending WRSR instruction code→ Status Register data on D→S# goes high.

Figure 6-4 Write Status Register (WRSR) sequence



Driving the Chip Select (S#) signal high at a byte boundary of the input data triggers the self-timed Write cycle that takes tW to complete (as specified in AC tables in: DC and AC parameters).

While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write in progress (WIP) bit: the WIP bit is 1 during the self-timed Write cycle tW, and 0 when the Write cycle is complete. The WEL bit (Write Enable Latch) is also reset at the end of the Write cycle tW.

The Write Status Register (WRSR) instruction enables the user to change the values of the BP1, BP0 and SRWD bits:

- The Block Protect (BP1, BP0) bits define the size of the area that is to be treated as read-only, as defined in Table 5-1.
- The SRWD (Status Register Write Disable) bit, in accordance with the signal read on the Write Protect pin (W#), enables the user to set or reset the Write protection mode of the Status Register itself, as defined in Table 6-3. When in Write-protected mode, the Write Status Register (WRSR) instruction is not executed. The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the tW Write cycle. The Write Status Register (WRSR) instruction has no effect on the b6, b5, b4, b1, b0 bits in the Status Register. Bits b6, b5, b4 are always read as 0.

Table 6-3 Protection modes

W#	SRWD bit	Mode	Status register
1	0	Software-protected	Status register is writable. the BP1 and BP0 bits can be changed
0	0		
1	1		
0	1	Hardware-protected	Status Register is Hardware write-protected. the BP1 and BP0 bits cannot be changed

The protection features of the device are summarized in Table 6-3. When the state register write inhibit bit (SRWD) in the state register is 0 (its initial transfer state), the state register can be written (provided that the WEL bit has previously set by the WREN statement) and write-protected (W#) The logic level applied to the input pin is irrelevant.

When the Status Register Write Disable (SRWD) bit in the Status Register is set to 1, two cases should be considered, depending on the state of the Write Protect (W#) input pin:

- If Write Protect (W#) is driven high, it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction).
- If Write Protect (W#) is driven low, it is not possible to write to the Status Register even if the WEL bit has previously been set by a WREN instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area, which are Software-protected (SFP) by the Block Protect (BP1, BP0) bits in the Status Register, are also hardware-protected against data modification Regardless of the order of the two events.
- the Hardware-protected mode (HDP) can be entered by:
- either setting the SRWD bit after driving the Write Protect (W#) input pin low,
- or driving the Write Protect (W#) input pin low after setting the SRWD bit.

Once the Hardware-protected mode (HDP) has been entered, the only way of exiting it is to pull high the Write Protect (W#) input pin.

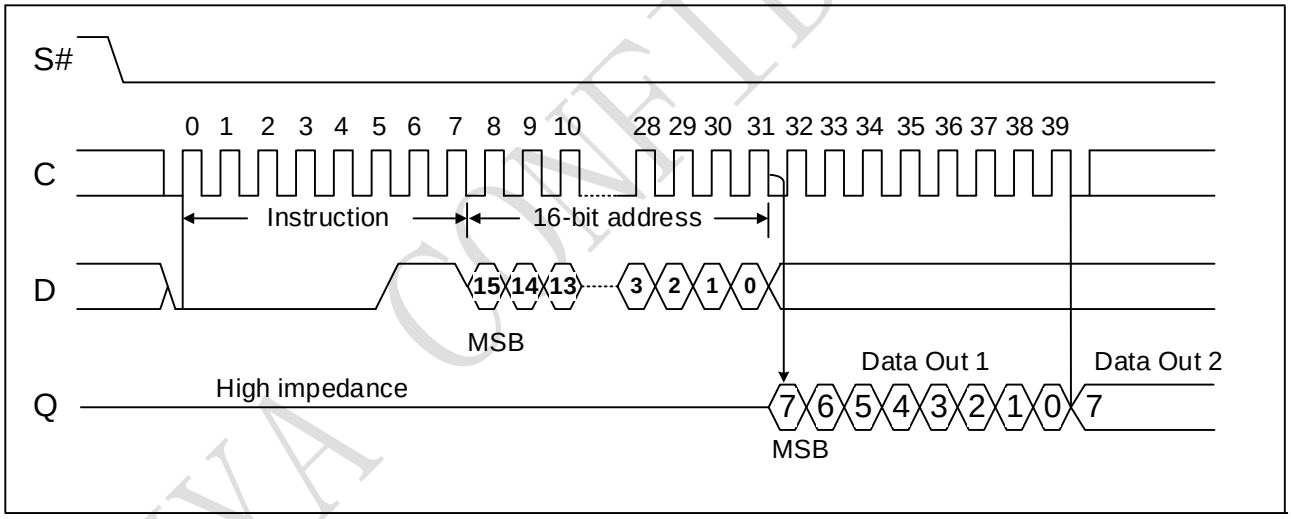
If the Write Protect (W#) input pin is permanently tied high, the Hardware-protected mode (HDP) can never be activated, and only the Software-protected mode (SFP), using the Block Protect (BP1, BP0) bits in the Status Register, can be used.

6.5 Read from Memory Array (READ)

The read instruction is for reading data out. The address is latched on rising edge of C, and data shifts out on the falling edge of C at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

As shown in Figure 6-5, the sequence of issuing READ instruction is: S# goes low→ sending READ instruction code→ 2-byte address on D→ data out on Q→ to end READ operation can use S# too high at any time during data out.

Figure 6-5 Read from Memory Array (READ) sequence



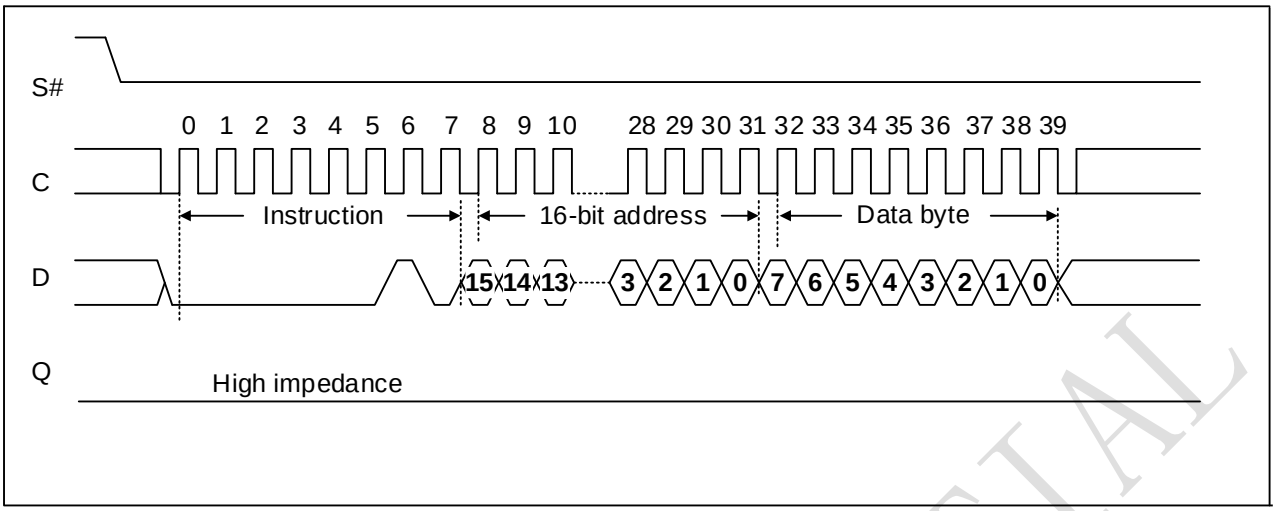
The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

6.6 Write to Memory Array (WRITE)

As shown in Figure 6-6, to send this instruction to the device, Chip Select (S#) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select (S#) high at a byte boundary of the input data. The self-timed Write cycle, triggered by the Chip Select (S#) rising edge, continues for a period tW (as specified in AC characteristics in DC and AC parameters), at the end of which the Write in Progress (WIP) bit is reset to 0.

Figure 6-6 Byte Write (WRITE) sequence



Note：

1.The self-timed write cycle tW is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)].

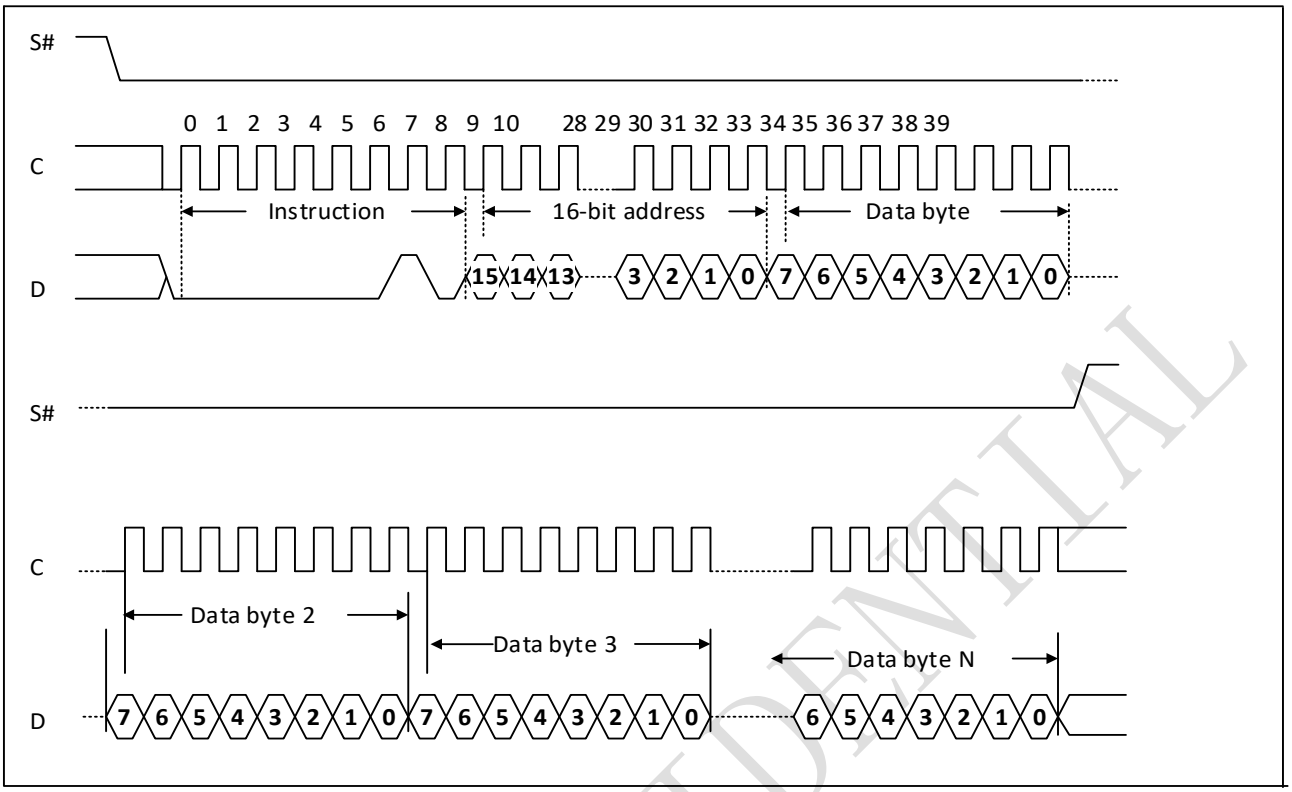
In the case of Figure 6-6, Chip Select (S#) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. However, if Chip Select (S#) continues to be driven low (as shown in Figure 6-7), the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle.

Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If more bytes are sent than will fit up to the end of the page, a condition known as “roll-over” occurs. In case of roll-over, the bytes exceeding the page size are overwritten from location 0 of the same page.

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before),
- if a Write cycle is already in progress,
- if the device has not been deselected, by driving high Chip Select (S#), at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in),
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

Figure 6-7 Page Write (WRITE) sequence



6.6.1 Cycling with Error Correction Code (ECC)

P25C08H devices offer an Error Correction Code (ECC) logic. The ECC is an internal logic function transparent for the SPI communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes[1] . Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group[1]. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the four bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value.

Note: [1] A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer

7. Power-up and delivery state

7.1 Power-up state

After power-up, the device is in the following state:

- Standby mode
- deselected (after power-up, wait 100us after V_{cc} min voltage, a falling edge is required on Chip Select (S#) before any instructions can be started).
- not in the Hold condition
- the Write Enable Latch (WEL) is reset to 0
- Write in Progress (WIP) is reset to 0

The SRWD, BP1 and BP0 bits of the Status Register are unchanged from the previous power-down (they are non-volatile bits).

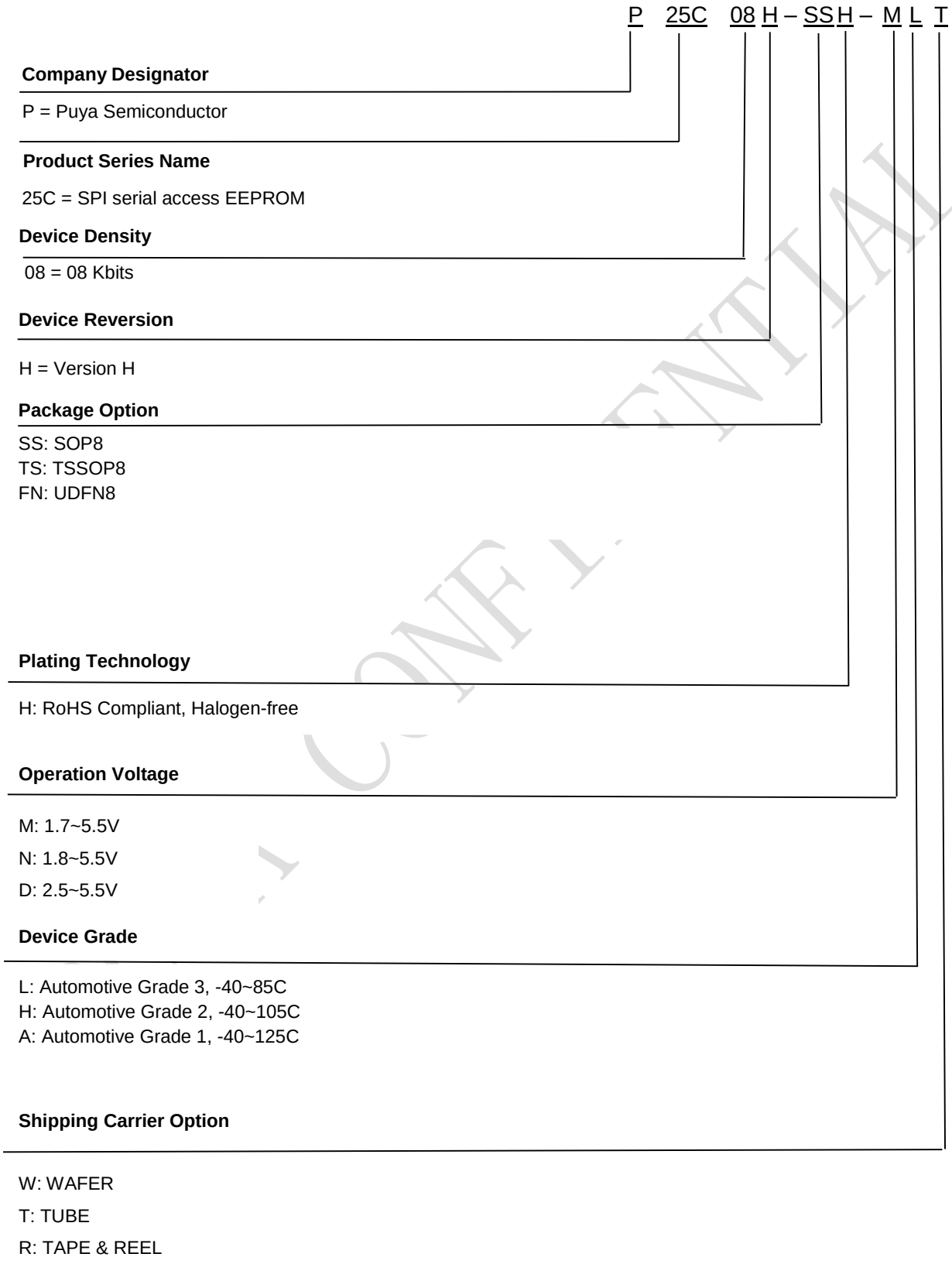
7.2 Initial delivery state

The device is delivered with the memory array and Identification Page bits set to all 1s (each byte = FFh).

The Status Register Write Disable (SRWD) and Block Protect (BP1 and BP0) bits are initialized to 0.

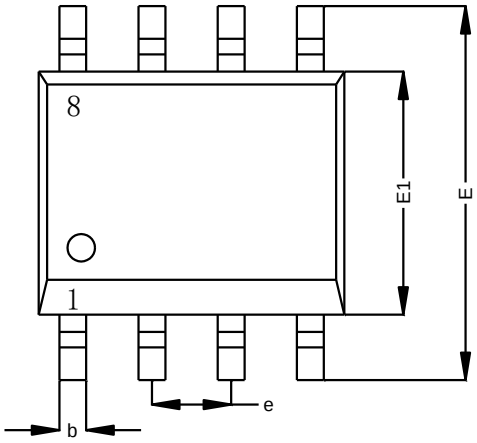
8. Ordering Code Detail

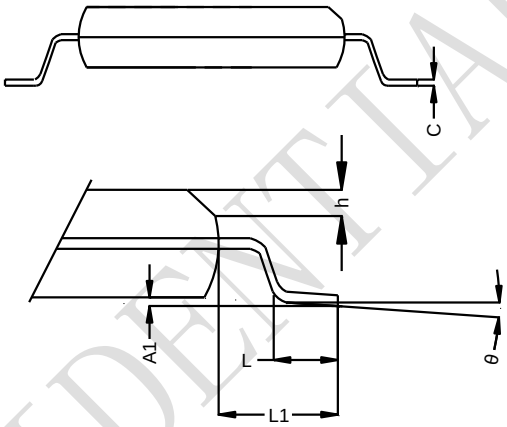
Example:

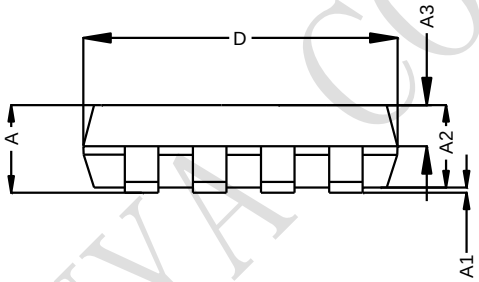


9. Package information

9.1 SOP8







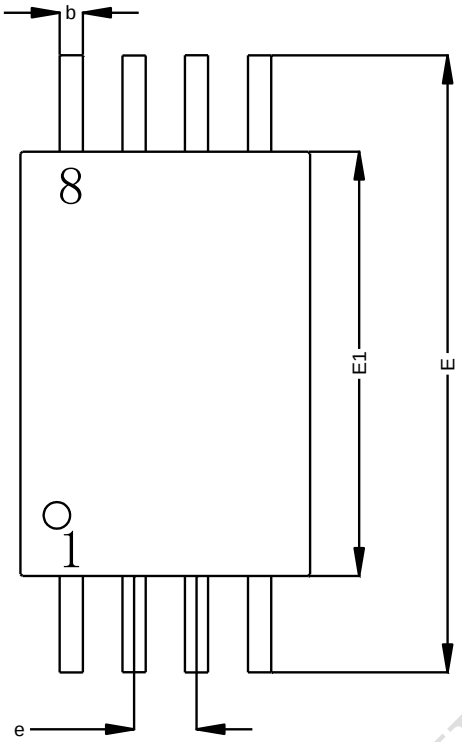
Common Dimensions
(Unit of Measure=millimeters)

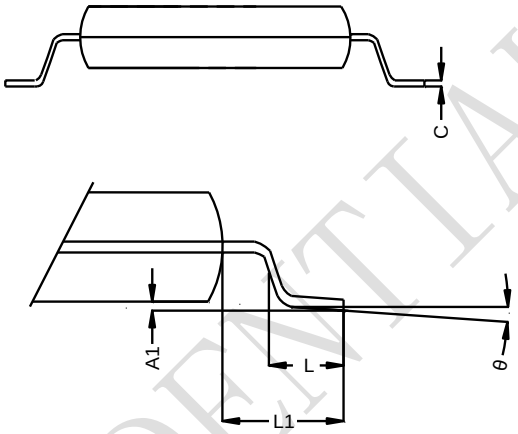
Symbol	Min	Typ	Max
A	-	-	1.750
A1	0.100	-	0.250
A2	1.250	-	-
b	0.310	-	0.510
c	0.170	-	0.250
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	-	1.270	-
L	0.400	-	1.270
L1	-	1.050	-
θ	0	-	8°
h	0.25	-	0.50

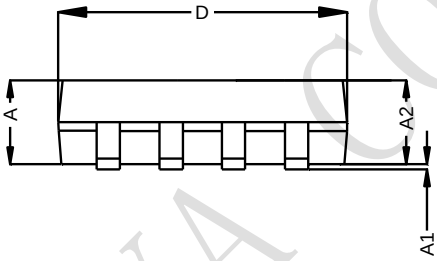
Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya SOP8（150mil）POD	QRPD-0004	1.0

9.2 TSSOP8







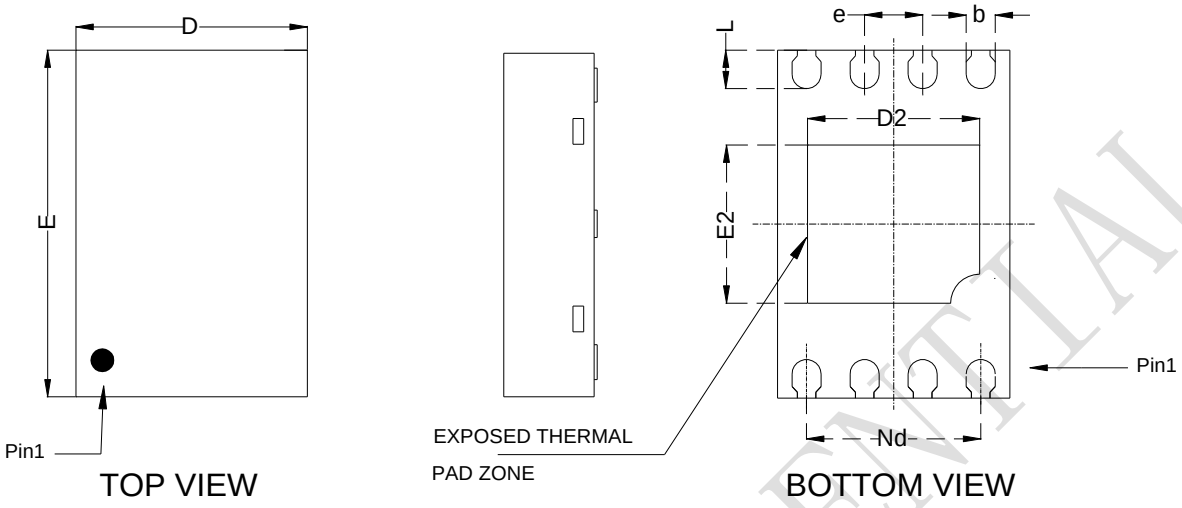
Common Dimensions
(Unit of Measure=millimeters)

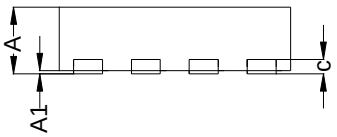
Symbol	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	1.000	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	2.900	3.000	3.100
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e	-	0.650	-
L	0.450	-	0.750
L1	-	1.000	-
θ	0	-	8°

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	PUYA TSSOP8 POD	QRPD-0019	1.0

9.3 UDFN8





SIDE VIEW

Common Dimensions

(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	–	1.50
E	2.90	3.00	3.10
E2	1.20	–	1.40
e	–	0.50	–
L	0.25	–	0.35
c	0.10	0.15	0.20
Nd	–	1.50	–

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya UDFN8L 2x3X0.5-0.5PITCH POD	QRPD-0025	1.0

10. Revision History

Version	Content	Date
Rev 1.0	Initial Release	2022-10-07
Rev 1.1	Update parameter of V_{IL}	2022-12-01
Rev 1.2	1） Update note in DC Characteristics 2） Update Features	2023-02-02
Rev 1.3	Update Features and Table 4-5	2024-02-01

Puya Semiconductor Co., Ltd.